REMARKS

Claims 2–14, 16-20, 22–40, 44–48 and 50–59 are pending in the application from which claims 7, 10, 12–14, 19, 22, 24–40, 48, 50–52 and 55 were withdrawn from consideration. Claims 2-6, 8-9, 11, 16-18, 20, 23, 44–47, 53-54, and 56–60 are reported as under consideration in the Office Action.

Applicants would like to thank the Examiner for the interview on April 6, 2004. The applicants would also like to thank Examiner Chris Chu for agreeing to withdraw the restriction requirement between Group I including claims 1-26 and 41-54 and Group II which includes claims 27-40 and claim 55. As agreed during the Examiner interview, the claims in Groups I and II are so closely related that the search of the claims in Groups I and II would not be a burden, especially in light of the amended claims. Accordingly, claims 27-42 and 55 are reinstated by amendment and listed as previously presented.

Finally, Applicants amend the description of the drawings on page 2 of the specification in order to show that at least two different embodiments are described in FIGS. 2-9, rather than a mere single embodiment.

Claim rejection 35 U.S.C. § 102(b)

Claims 5, 6, 8, 9, 44, 46, 47, 56 and 58 are rejected under 35 U.S.C. § 102(b) based on Tanioka.

Tanioka

Tanioka is directed to a multichip module having wiring layers on front and back surfaces. (Col. 3, lines 54–57.) A carrier board 3 disposed at the back surface of the multichip module includes pads for external connection. (Col. 3, line 67–Col. 4, line 11.) By changing the pad arrangement to a matrix arrangement, the spacing between the external connection terminals reduces solder flowing between pads, thus increasing yield. (Col. 5, lines 33–37.) A silicon

layer 9 is interposed between the MCM board 1 and the carrier board 3 to enable cooling of the bare chip. (Col. 5, lines 9–10; Col. 5, lines 41–43.)

The Office Actions dated March 1, 2004 and October 24, 2003 allege that Tanioka discloses an unpackaged semiconductor die 2 (FIGS. 2A-2C) directly attached to the package module, the unpackaged semiconductor die encapsulated 16 (FIG. 2A) onto the package module in a structure having a planar top surface. The Office Action also alleges that, as illustrated in a drawing reproducing FIG. 2A of Tanioka, Tanioka discloses a packaged semiconductor die (17) having a top surface and attached to the package module of equal height. However, the drawing reproduced in the Office Action inaccurately indicates the proper alignment of the top surface of the semiconductor (17) and the unpackaged semiconductor (2). A corrected drawing of FIG. 2A showing the top surfaces is provided at the end of this response. As illustrated in FIG. 2A, attached at the end of this response, the top sides of the unpackaged semiconductor (2) and of the packaged semiconductor (17) are not of equal distance from the package module.

Independent Claim 56

Independent claim 56 recites, among other features, "the . . . unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate."

The Office Action, relying solely on FIGS. 2A-2C of Tanioka, asserts that FIGS. 2A–2C of Tanioka describe the elements of Claim 56. As stated above, according to FIG. 2A in Tanioka, the small outline package 17 on both the left and to the right is shown to rise to a height that is less than the height of a neighboring package module 2. For at least the reasons stated below, FIGS. 2A-2C are unlike Applicants' claimed subject matter reciting, inter alia, an

"encapsulated . . . structure having a planar top surface . . . wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." (Claim 56.)

According to the Final Office Action dated March 1, 2004, the Office Action acknowledges the drawing appended to the Office Action dated December 1, 2003 showing a corrected figure FIG. 2A drawing. However, without explaining how the corrected drawing of FIG. 2A is deficient, the Office Action in a conclusory manner simply continues to assert that the distances in issue are "of equal distance from the substrate." The Office Action not only fails to show how the corrected drawing provided in the previous response is deficient but provides no reasons whatsoever for drawing a line labeled A to pass below the edge of semiconductor (17) on the left side of FIG. 2A, to pass through the unpackaged semiconductor (2) and again to pass through the edge of semiconductor (17) rather than along the outside edge. Rather than showing the lines consistently along the outside edge of each of the packaged semiconductor dies (17) and the encapsulated structure (2), as shown in the drawing attached to the previous Office Action Response, the Office Action shows a line going through rather than outside of the unpackaged semiconductor (2) and through the semiconductor (17). As such, the Office Action attempts to modify Tanioka by running a line through semiconductors (2) and (17), in an unsuccessful reading on the claims.

For example, if the line A represented the edge of a heat sink, the heat sink, as drawn in the Office Action, would have to cut into and go through the unpackaged semiconductor (2) and the semiconductor (17) on the right side of the figure, an impossibility as shown. Since the Office Action fails to address the arguments previously presented in the Response dated December 1, 2003, the Office Action simply ignores the arguments previously presented since

no reason and no argument is presented to counter the Applicants' previous arguments. In contrast, the Applicants did provide and further provide several arguments and several additional reasons for showing that the line A, as drawn in the Office Action, is incorrect as it goes through the unpackaged semiconductor (2) and the semiconductor (17), rather than along the outside edge of the unpackaged semiconductor (2) and the semiconductor (17). Further, the Office Action fails to address the gaps shown as arrows pointing towards each other in the figure attached to the previous Office Action, showing a gap formed between the line along the outside edge of unpackaged semiconductor (2) and the top surface of semiconductor (17) on both the left and right side. As such, the Office Action mischaracterizes Tanioka and ignores a principal element of the claims. Additionally, the Office Action merely attempts to improperly amend Tanioka in an effort to read on the claims. Therefore, the Office Action fails to show how Tanioka teaches each and every element as arranged in Claim 1.

Therefore, with regard to the assertion in the Office Action that the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate, a careful examination of the line A drawn in the Office Action with respect to FIG. 2A does not appear to be properly aligned with both the top surfaces of the packaged semiconductor dies (17) and the encapsulated structure (2). Rather, Applicants submit the attached drawing at the end of this response shows more accurately drawn lines from the top surface of encapsulated structure (2) and the top surfaces of the packaged semiconductor dies (17), as shown on the left side of FIG. 2A and the right side of FIG. 2A. The lines provided in the revised drawing clearly show that the planar top surface of the encapsulated structure (2) and the top surface of the packaged semiconductor die (17) are not of equal distance from the substrate. For example, the line A in the drawing of FIG. 2A in the Office Action is not properly

aligned with the top surface of the encapsulated structure (2). For example, the Applicants cannot find where Tanioka describes attaching a heat sink to the printed circuit board 19 in FIG. 2A. Clearly, Tanioka never contemplated the planar top surface of the encapsulated structure (2) and the top surface of the packaged semiconductor die (17) being of equal distance from the substrate.

The Office Action dated March 1, 2004 on page 10 makes reference to the Applicant's specification as amended on February 28, 2002 on page 2, lines 5 through 15.

> FIG. 6 illustrates a heat sink 150 added on top of unpackaged semiconductor die 110 and packaged die 120 and 130 to aid in removing heat from the circuits. As illustrated, the distance "D" from the top of multi-die modules substrate 140 to the top of packaged die 120 and 130 is substantially equal to the distance on the top of multi-die modules substrate 140 to the top of the encapsulation material over unpackaged semiconductor die 110, which is referred to herein as the top of unpackaged semiconductor die 110. In at least one embodiment, distance "D" is about 1.3 millimeters. Making these distances the same facilitates effective use of heat sink 150, although heat sink 150 could be fabricated to account for any difference between the heights of various packaged and/or package that the upper hand and/or unpackaged die attached or monitored through multi-die module substrate 140. In various embodiments, heat sink 150 may be a thin strip of heat conductive material, enlarged heat sink with fins for added heat dissipation, or any other suitable type of heat sent.

The Applicants would like to note that the Office Action appears to quote from the Applicant's specification; however, the quotation in the Office Action omits material portions from the entire paragraph, namely the very first sentence referring to a heat sink 150 added on top of unpackaged semiconductor die 110 and packaged die 120 and 130 to aid in removing heat from the circuits. As such, the discussion in the following sentence with regard to the distance of "D" according to one embodiment from the top of multidie module substrate 140 to the top of package die 120 and 130 being substantially equal to the distance from the top of multidie module substrate 140 to the top of the encapsulation material over unpackaged semiconductor

die 110 makes reference to the distance "D" immediately upon making reference to the heat sink 150 added on top of unpackaged semiconductor die 110 and packaged die 120 and 130. As a result, the Office Action ignores the context of the discussion with regard to the distance "D", according to one embodiment, namely to facilitate a heat sink. Further, the Office Action ignores yet another material portion of the quoted sentence, which states "making these distances the same facilitates effective use of heat sink 150," which relates the distances to facilitate the effective use of the heat sink 150. The omission of this portion of the sentence, which links the distances referred to above in order to facilitate effective use of the heat sink 150, ignores a principal portion of the specification as cited and, as a result, improperly mischaracterizes the Applicants' specification. As will be discussed in more detail further below, the application of the heat sink to the unpackaged semiconductor (2) in FIG. 2A of Tanioka would result in a gap between the planar heat sink and the top surface of semiconductor (17) both on the left and right side of FIG. 2A of Tanioka, resulting in reduced conduction of heat. The application of the planar heat sink (2) unpackaged semiconductor (2) further illustrates that the line A, as drawn in the Office Actions both mailed on October 24, 2003 and December 1, 2003, illustrates how the line drawn in the Office Action mischaracterizes Tanioka. Further, the attempt to modify Tanioka illustrates how Tanioka precludes the application of a heat sink to unpackaged semiconductor (2), since line A is not drawn on the outside surface of unpackaged semiconductor (2) but actually goes through the protective resin (16) (shown as dotted material).

As such, the line A drawn through the encapsulation material (16) leaves one to wonder if the Office Action requires some type of shaving removal, or displacement of the encapsulation material in order to accommodate line A passing through the outer top surface of semiconductors (17) and unpackaged semiconductor (2) so that the line is on the same plane. At any rate, the

Office Action clearly would require some type of modification to Tanioka in order to accommodate a heat sink to both the unpackaged semiconductor (2) and the semiconductor 17 on both the right and left side.

Additionally, if one were merely to attach a heat sink to the unpackaged semiconductor 2, then the resultant gap between the planar inside surface of the heat sink and the outer top surface of left and right semiconductors (17) would prevent effective dissipation of the heat generated in the semiconductor (17), since no direct contact would occur between the outer top surface of the semiconductor (17) and the inside surface of a planar heat sink. Therefore, the very language in the specification that the Office Action merely ignores ("making these distances the same facilitates effective use of heat sink 150") provides the appropriate context between the distances, as discussed in the specification. The assertion in the Office Action on page 10 that "the term 'of equal distance' is defined as not exactly equal distance" ignores the language "making these distances the same facilitates effective use of heat sink 150" and, therefore, at least for this reason, mischaracterizes the specification. The Applicants traverse the assertion made in the Office Action that the term "of equal distance" is defined as not exactly equal distance for at least the reason stated above and also for at least the reason stated below.

According to the Office Action on page 11, the Applicants merely argue the advantages present in Applicants' claimed subject matter rather than pointing out specific special differences. However, the advantages, as previously described, are directly related to these structural differences between the claim and recited portions of Tanioka. Further, the advantages, as referred to by the Office Action, are directly related to the distances that facilitate effective use of the heat sink according to one embodiment. The relation of the distances to facilitate an effective use of the heat sink is precisely the language ignored in the block quote at

the bottom of page 10 in the Office Action. Further, the omission of a material portion of the specification from a block quote on the bottom of page 10 further illustrates that the Office Action mischaracterizes the specification, as well as the claims. Further, rather than addressing the relation of the distances from the top of multidie module substrate 140 to the top of package die 120 and 130 to facilitate effective use of heat sink 150, the Office Action simply chooses to ignore that portion of the specification and, as a consequence, fails to affirmatively show the distances from the top of the multidie module substrate 140 to the top of package die 120 and 130 do not facilitate effective use of the heat sink 150.

As previously stated, Applicants submit that the encapsulation design of Tanioka lacks the advantages present in Applicants' claimed subject matter. For example, Applicants' planar top surface of an encapsulation structure is positioned in a coplanar fashion relative to the top portion of a neighboring package module, such that a heat sink having a planar bottom (e.g., a simple universal design) can be placed on top of both the top surface of the encapsulation structure and on the top portion of a neighboring package module. As a result, the heat sink in the claim's configuration is in contact with both items and rests upon a relatively large portion of both items, where the large contact between both the encapsulation structure and the neighboring package module and the heat sink allows for significant heat transfer from both items to the heat sink. In contrast, the encapsulation design disclosed in Tanioka is less desirable than Applicants' claimed subject matter because, rather than dissipate heat with a heat sink, Tanioka applies a silicon layer to enable cooling of the bare chip. Further, when a heat sink having a planar surface is placed on top of both the packaged and encapsulated semiconductor dies having different heights, such a heat sink then assumes an angled position across the two items. In such a position, the heat sink only contacts the edge of the packaged heat sink and only a point of the

dome, i.e., as shown in FIGS. 1, 3 in Tanioka of the encapsulated material. As such, the resulting heat transference is relatively small and the physical connection to the heat sink is positioned on an undesirable angle, resulting in a number of disadvantages. It should be also noted that, regardless of the height of the top surface of the domed-shaped encapsulated structure, any heat sink with a planar surface in contact with devices of different heights only shares a small contact position therewith and, as such, will result in a relatively poor transference of heat there between.

Additionally, rather than teaching a heat sink, Tanioka teaches a silicon layer 9 interposed between the MCM board 1 and the carrier board 3 to enable cooling of the bare chip. (¶ 5, lines 9–10; ¶ 5 lines 41–43.) Since Tanioka teaches cooling of the bare chip with the silicon layer 9, Tanioka teaches away from contacting a coplanar heat sink surface and therefore teaches away from a planar top surface of an encapsulation structure positioned in a coplanar fashion with the neighboring package module. Since Tanioka teaches a totally different and less effective form of heat dissipation, the solution taught by Tanioka is unsatisfactory and therefore teaches away from the claims. Applicants submit that the encapsulation design of Tanioka fails to teach each and every element arranged in the claims and further lacks these and other advantages present in Applicants' claimed subject matter.

Another example of such an advantage includes in one exemplary embodiment that Applicants' metal cap encapsulation technique provides the advantages associated with the properties of metallic structures generally and, more specifically, for some embodiments, the presence of a gap between the enclosed die and surrounding metal cap structure itself. In contrast, the silicon layer 9 interposed between the carrier board 3 and the MCM board 1, as taught by Tanioka, is less desirable than Applicants' claimed subject matter since the silicon

layer does not dissipate heat as does a heat sink and, therefore, does not require the planar surface and does not provide the properties, such as heat transfer, provided by Applicants' claimed subject matter, nor is such material a metal cap, as acknowledged in the Office Action.

Applicants submit that nowhere does Tanioka teach the claim limitation "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Because Applicants can identify no language in Tanioka as cited that makes reference to the height of the packages, and because Tanioka teaches mounting a carrier board 3 directly to the package modules rather than a heat sink and, further, because FIG. 2 as cited shows the small outline package 17 rises to a height that is less than the height of a neighboring package module 2, Applicants submit that Tanioka does not disclose Applicants' claimed subject matter, but further teaches away from Applicants' invention. Therefore, Applicants request a respective showing of all the elements as arranged in the Claims. As such, it is respectfully submitted that claim 56 is allowable as written.

Applicants submit that Tanioka does not disclose, teach or suggest claim 56's language including, inter alia, "an . . . unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and a packaged semiconductor die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Nor does Tanioka disclose, teach or suggest the subject matter of claim 56 as a whole. Applicants submit that, at least for the reason that Tanioka discloses an encapsulated structure covered by a carrier board 3 where such structure is shown as being located at a position having a height different than of a neighboring package module, independent claim 56 is neither anticipated, nor is it obvious in view of Tanioka.

Independent Claim 57

Independent claim 57 recites, among other features, "a . . . graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate."

Applicants respectfully reassert the arguments made above regarding the failure of Tanioka to teach the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate. Further, Applicants submit that Tanioka does not disclose, teach or suggest, claim 57's language including, inter alia, "a . . . graphics-processing die encapsulated on the package module in a structure having a planar top surface; and a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the substrate," nor does Tanioka disclose, teach or suggest the subject matter of claim 57 as a whole. Applicants submit that, at least for the reasons that Tanioka discloses an encapsulated structure covered by a carrier board 3, where such structure is shown as being located at a position having a height different than of a neighboring package module, independent claim 57 is neither anticipated, nor is it obvious in view of Tanioka.

The Office Action dated March 1, 2004, asserts that the semiconductor module "sized to be interchangeable with standard package sizes" employs intended use language. Further, the Office Action states that the argument previously presented "is not persuasive since Tanioka's packaged module is capable of performing the intended use language, [as such] Tanioka meets

the claim." However, the assertion of the intended use standard established in the Office Action is not consistent with the standard established by the Federal Circuit.[1] "The court stated that the phrase 'so dimensioned' is as accurate as the subject matter permits, noting that the patent law does not require that all possible lengths corresponding to the spaces in hundreds of different automobiles be listed in the patent, let alone that they be listed in the claims." Accordingly, since the language "so dimensioned" in the case is analogous to claim 57, namely the claim language "a package module sized to be interchangeable with standard package sizes" (see M.P.E.P. § 2173(b) 1.05), the language in claim 57 is sufficiently accurate and, therefore, the rejection is improper. Further, the standard asserted in the Office Action that "Tanioka's packaged module is capable of performing the intended use language, [as such] Tanioka meets the claim," is unsupported and conclusory. Additionally, the Office Action stated that Tanioka's packaged module is capable of performing the intended use language rather than the Applicants' claimed language. Further, the Office Action improperly asserts the standard established by the Federal Circuit by stating that Tanioka's packaged module is capable of performing the intended use language rather than showing or providing any reason for the assertion that claim 57 language is intended use language. As previously stated, the claim language "sized to be interchangeable with standard package sizes" is as accurate as the subject matter permits, knowing that the patent law does not require that all possible language be listed in the patent, let alone that they be listed in the claims. For example, the subject matter, multidie modules, permits the language "sized to be interchangeable" with standard package sizes since the referenced size is referenced with respect to known standard package sizes. The Office Action provides no reason why standard package sizes would not be understood in this subject matter.

[1] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1 U.S.P.Q.2d 1081 (Fed. Cir. 1986), *see also* M.P.E.P. §2173.05(b).

Further, the Office Action fails to provide any type of basis or any other argument for the assertion that the claim language "sized to be interchangeable with standard package sizes" employs intended use language.

Independent Claim 58

Independent claim 58 recites, among other features, an unpackaged semiconductor die encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

The Office Action repeats essentially the above rejection without any additional arguments or any additional reasons or basis for the rejection. Since the Office Action fails to provide a sufficient basis for the rejection, as previously stated above, the Office Action fails to show how Tanioka anticipates claim 58 or any other claim for that matter.

Applicants respectfully reassert the arguments made above regarding Tanioka. Further, Applicants submit that Tanioka does not disclose, teach or suggest claim 58's language including, inter alia, "an unpackaged semiconductor die . . . encapsulated in a structure having a planar top surface; and a packaged semiconductor die having a top surface and mounted on the first surface of the substrate; wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate," nor does Tanioka disclose, teach or suggest the subject matter of claim 58 as a whole. Applicants submit that, at least for the reasons that Tanioka as cited discloses an encapsulated structure covered by a carrier board 3 where such structure is shown as being located at a position having a height different from that of a neighboring package module, Tanioka teaches away from the claims. Therefore, independent claim 58 is neither anticipated nor obvious in view of Tanioka.

Dependent Claims 3 and 4

Applicants respectfully reassert the arguments made above regarding the above claims. In addition, Applicants also submit that, because claims 3 and 4 depend from claim 56 and, as dependent claims therefrom, claims 3 and 4 are allowable for at least the reasons claim 56 is allowable. As acknowledged in the Office Action, nowhere does Tanioka disclose, teach or suggest wherein the unpackaged semiconductor die is a graphics processor, or where the packaged semiconductor is a memory. As such, Tanioka does not disclose, teach or suggest Applicants' claimed subject matter. Applicants further submit, as argued in part at least immediately above, that claims 3 and 4 are also allowable in light of the presence of novel and non-obvious elements contained in claims 3 and 4 that are not otherwise present in claim 56. Additionally, pursuant to M.P.E.P. §2144.03, Applicants respectfully challenge the assertion that Tanioka "encompasses all well known semiconductor dies including a 'memory die'" as asserted with respect to each and every element as arranged in claims 3 and 4 and request that supporting reference be cited for each element of these claims if the rejection is maintained. Further, such an assertion contradicts the assertion that claim 57 uses intended use language for the reasons stated with respect to claim 57 and since the claim recites standard package sizes.

Dependent Claims 5 and 6

Applicants respectfully reassert the arguments made above regarding the above claims. In addition, Applicants also submit that claims 5 and 6 depend from claim 56, and as dependent claims therefrom, claims 5 and 6 are allowable for at least the reasons claim 56 is allowable. Applicants further submit, argued in part at least immediately above, that claims 5 and 6 are also allowable in light of the presence of novel and non-obvious elements contained in claims 5 and 6 that are not otherwise present in claim 56.

Dependent Claims 8 and 20

Applicants respectfully reassert the arguments made above regarding claims 56 and 57, respectively. In addition, Applicants also submit that, because claims 8 and 20 depend from claims 56 and 57 respectively and, as dependent claims therefrom, claims 8 and 20 are allowable for at least the reasons claims 56 and 57 are allowable. Applicants further submit, argued in part at least immediately above, that claims 8 and 20 are also allowable in light of the presence of novel and non-obvious elements contained in claims 8 and 20 that are not otherwise present in claims 56 and 57. Although the Examiner asserts that the burden of proof is on the Applicants, the burden of proof for establishing a *prima facie* case of anticipation and obviousness rests on the Examiner, not on the Applicants.[2] Since the Examiner has not established a prima facie case of anticipation or obviousness, the rejections are improper.

Dependent Claim 9

Applicants cannot find where Tanioka as cited does not disclose, teach or suggest, either explicitly or implicitly, Applicants' claim, inter alia, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die. (Claim 9.) As such, Applicants respectfully submit that Tanioka does not disclose, teach or suggest Applicants' claimed subject matter of claim 9.

Dependent Claims 17 and 18

Applicants respectfully reassert the arguments made above regarding claim 57. In addition, Applicants also submit that, because claims 17 and 18 depend from claim 57, therefore, dependent claims 17 and 18 are allowable for at least the reasons claim 57 is allowable. Applicants further submit, argued in part at least immediately above, that claims 17 and 18 are

[2] See M.P.E.P. §2142 and case citations therein.

also allowable in light of the presence of novel and non-obvious elements contained in claims 17 and 18 that are not otherwise present in claim 57.

Dependent Claims 44, 45, 46, 47, 53 and 54

Applicants respectfully reassert the arguments made above regarding claim 58. In addition, Applicants also submit that, because claims 44, 45, 46, 47, 53, and 54 depend from claim 58, therefore, dependent claims 44, 45, 46, 47, 53, and 54 are allowable for at least the reasons claim 58 is allowable. Applicants further submit, argued in part at least immediately above, that claims 44, 45, 46, 47, 53, and 54 are also allowable in light of the presence of novel and non-obvious elements contained in claims 44, 45, 46, 47, 53, and 54 that are not otherwise present in claim 58.

Claim rejection 35 U.S.C. 103

Claims 2, 16, and 45

Claims 2, 16, and 45 are rejected under 35 U.S.C. §103(a) under Tanioka in view of Fallon, et al.

It is well-established that to establish *prima facie* obviousness, all the claim limitations must be taught or suggested by the prior art. In addition, there must be some teaching, motivation or suggestion, in either the prior art or the references themselves, to make the combination asserted by the Examiner. In reviewing the Office Action, the Examiner asserts "it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using a ball grid array package for the packaged semiconductor as taught by Fallon, et al." and "The ordinary artisan would have been motivated to modify Tanioka in the manner described above *for at least the purpose of increasing a bond strength* between the packaged semiconductor and the substrate." (Emphasis added.) Contrary to the assertion of the Office Action that the ball grid array package would increase the bond strength between the

packaged semiconductor and the substrate, Fallon describes the use of bond wire (868), such as aluminum, "extends between each wire bond pad of the chip and a corresponding wire bond pad (870) on coupling surface (872) of the attachment substrate (874)." (Fallon, et al. ¶37, lines 59-64.) "Connectors (878) are located on the bottom surface of the carriers or modules of the invention." *Id.* Accordingly, the assertion that the ball grid array increases the bond strength between the packaged semiconductor and the substrate is contrary to, or at least unsupported by, the teachings of Fallon, which instead teaches the use of bond wire (868).

Further, the Office Action provides no support for the assertion that the use of a ball grid array package could be used for "increasing a bond strength between the packaged semiconductor and the substrate." Additionally, the Office Action fails to describe relative to what the ball grid array increases the bond strength with, i.e., does the ball grid array increase bond strength relative to bond wires? If so, no support for such an assertion is provided and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

Measuring a claimed invention against the standard established in §103 requires the difficult but critical step of casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references in the then-accepted wisdom in the field.[3] Close adherence to this methodology is especially important in the case of less technologically complex inventions, where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher."[4]

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[3] *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).

[4] *Id.*

Case law makes it clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.[5] Combining prior art references without evidence of such a suggestion, teaching or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[6] Evidence of a suggestion, teaching or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, although "the suggestion more often comes from the teachings of the pertinent references."[7] ("The Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select the references and combine them.")

The showing of such suggestion, teaching, or motivation must be clear and particular.[8] Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."[9] As previously stated, the Office Action asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamioka by using the ball grid array package for the packaged semiconductor, as taught by Fallon. With regard to the Examiner's assertion of the motivation of one skilled in the art to modify the system of

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[5] *In re Dembiczak*, 50 U.S.P.Q.2d 164, 167 (Fed. Cir. 1999).

[6] *Id.*; see, e.g., *Interconnect Planning Corp. v. File*, 774 F.2d 1132, 1138, 227 U.S.P.Q. 543, 547 (Fed. Cir. 1985).

[7] *Dembiczak*, 50 U.S.P.Q.2d 164, 167 (Fed. Cir. 1999); *In re Roffet*, 149 F.3d 1350, 1359, 47 U.S.P.Q. 2d 1453, 1459 (Fed. Cir. 1998)

[8] *Dembiczak*, 50 U.S.P.Q.2d 164, 167 (Fed. Cir. 1999); see, e.g., *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352, 48 U.S.P.Q.2d 1225, 1232 (Fed. Cir. 1998).

[9] *Dembiczak*, 50 U.S.P.Q.2d 164, 167 (Fed. Cir. 1999); see, e.g., *Elmurry v. Arkansas Power & Light Co.*, 995 F.2d 1576, 1578, 27 U.S.P.Q.2d 1129, 1131 (Fed. Cir. 1993); *In re Sichert*, 566 F.2d 1154, 1164, 196 U.S.P.Q. 207, 217 (C.C.P.A. 1977).

Tanioka, a careful examination of Tanioka and Fallon, as cited, reveals that Fallon instead teaches the use of bond wires rather than the ball grid array asserted in the Office Action. Accordingly, taken in the proper context, Fallon teaches the avoidance of the use of a ball grid array package, but rather the use of a bond wire (868) between each wire bond pad of the chip in the corresponding wire bond pad (870) of a coupling surface (872) of an attachment substrate (874). (Fallon ¶37, lines 59–63.) Additionally, as previously stated, the Office Action dated March 1, 2004, provides no support whatsoever for the assertion that the ball grid array package increases bond strength between the packaged semiconductor and the substrate. Accordingly, the Applicants challenge such an assertion, pursuant to M.P.E.P. §2144.03. The Applicants further note that the Office Action dated March 1, 2004 on pages 13, 14 and 15 fails to provide the support for the assertion that the ball grid array package increases bond strength between the packaged semiconductor and the substrate in response to the challenge to such assertion in the previous response. As such, for at least these reasons, the Office Action dated March 1, 2004 fails to address each and every one of the Applicants' arguments and, as such, the Applicants continue to request a showing of each and every element as arranged in the claims. The Office Action on page 14 asserts that since Fallon also teaches in FIG. 46 "the bumped module of the invention, the motivation [is] not contrary to the teachings of Fallon." However, the Office Action completely fails to address the arguments made in the previous response, including those referring to portion of Fallon at ¶37, lines 63 through 64, which state "preferably, the wire bond chip, bond wires and coupling pads are encapsulated with an organic material 876."

Further the Office Action asserts that "since the total attached area of [the] ball grid array is more than the total attached area of wire bond, the ball grid array [increases] bond strength relative to bond wires." However, no support, reason or any argument is provided to support

such an assertion since the bond strength may be related to more than just the area, such as, for example, the adhesive qualities between two objects. Accordingly, the Applicants challenge such an assertion, pursuant to M.P.E.P. §2144.03.

Additionally, Tanioka teaches away from the claims because, among other things, Tanioka teaches mounting a carrier board 3 directly to the package modules rather than a heat sink and, therefore, Tanioka teaches away from "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." As stated in the response to the Office Action dated January 1, 2003, Fallon teaches an encapsulation material as only having an arc or dome shape and, therefore, also teaches against "wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate." Since both Tanioka and Fallon teach away from the claims, there is no motivation to combine the references to produce the claimed invention.[10] Without the presence of any such motivation to combine such references to produce Applicants' invention, the later suggestion to combine such references is impermissible hindsight and, as such, is an invalid argument for a finding of unpatentability due to obviousness.

With regard to claim 45, the Office Action asserts Tanioka discloses the semiconductor package set forth in the claims except for plurality of the unpackaged semiconductor die mounted on the first surface of the substrate. The Office Action also asserts that one would be motivated to modify Tanioka in the manner described for at least the purpose of increasing power and speed of the module. However, the Office Action provides no support for how the

[10] A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983).) See M.P.E.P. §2141.02.

power and speed of the module would be increased by mounting the unpackaged semiconductor die on the first surface of the substrate. As previously stated, a broad conclusory statement standing alone is not evidence of motivation to combine. The Office Action merely has used the claims as a guide map to provide the motivation for the combination of Tanioka with Fallon. As a result, the Office Action fails to establish a *prima facie* case of obviousness.

Claims 3, 4, 17, 18, 20, 53, 54 and 57

Claims 3, 4, 17, 18, 20, 53, 54 and 57 are rejected under 35 U.S.C. §103(a) based on Tanioka in view of Hannah. Applicants respectfully reassert the arguments made above. In addition, Applicants also submit that these claims are allowable for at least the reason the independent claims are allowable. Applicants further submit, as argued in part at least immediately above, that these claims are allowable in light of the presence of novel and non-obvious elements. The Office Action asserts that the ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of receiving commands and graphics data from the main CPU of the computer. The Office Action fails to show how the argument that the receiving commands and graphics from a main CPU of the computer would provide any type of motivation for modifying Tanioka in view of Hannah. Without the presence of any such motivation to combine such references to produce Applicant's invention, the asserted suggestion to combine the references is impermissible hindsight and, as such, is an invalid argument for a finding of unpatentability due to obviousness.

With regard to claims 4 and 5, the Office Action states that the ordinary artisan would have been motivated to modify Tanioka in the manner described above for at least the purpose of decreasing cost. However, the Office Action does not show how using the semiconductor die decreases memory cost.

Claims 11 and 23

Claims 11 and 23 are rejected under 35 U.S.C. §103(a) under Tanioka in view of Takano, et al. Applicants respectfully reassert the arguments made above regarding claims 56 and 57. In addition, Applicants also submit that claims 11 and 23 depend from claims 56 and 57, respectively, and as a dependent claim therefrom, claims 11 and 23 are allowable for at least the reasons claims 56 and 57 are allowable. Applicants further submit, argued in part at least immediately above, that claims 11 and 23 are also allowable in light of the presence of novel and non-obvious elements contained in claims 11 and 23 that are not otherwise present in claims 56 and 57.

Independent Claim 59

Claim 59 is rejected under 35 U.S.C. §103(a) under Tanioka in view of DiStefano. Independent claim 59 recites, among other features, "an unpackaged semiconductor die . . . encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap." Applicants submit that neither Tanioka nor DiStefano, either in combination or individually, disclose, teach or suggest, claim 59's language including, inter alia, "an unpackaged semiconductor die . . . encapsulated in a structure; and a packaged semiconductor die mounted on the first surface of the substrate wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap." Further, Tanioka and DiStefano, either in combination or individually, fail to disclose, teach or suggest the subject matter of claim 59 as a whole.

On page 16 of the Office Action dated March 1, 2004, the Office Action asserts that the test for obviousness is not whether the features of the secondary reference may be bodily incorporated into the structure of the primary reference, nor is it that the claimed invention must

be expressly suggested in any one or all of the references. However, the previous response made no such assertion. The previous response as described below merely cites case law indicating that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, the teachings of the references are not sufficient to render the claims *prima facia* obvious. The case law and the M.P.E.P. states:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); see M.P.E.P. §2143.01.

Further, the Federal Circuit has held that if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification.[11] The Office Action provides no reason or explanation for any deficiencies in the cited case law and provides no reason or argument for stating how there is any contradiction between the case law as cited and *In re Kelliher* cited on page 16 of the Office Action dated March 1, 2004.

The Office Action acknowledges that "Tanioka does not disclose the encapsulating structure being further comprised of an encapsulating material of a metal cap." Additionally, DiStefano, as cited, requires that the cap 20 include "a pair of flanges 26 projecting outwardly from flanges 24 at the forward edges thereof, remote from rear wall 22." Such flanges on the metal cap of the encapsulating material would impermissibly interfere with the unpackaged semiconductor and, therefore, increase the surface area of the module. As a result, the suggestion to modify Tanioka with DiStefano would impermissibly change the principle of

[11] If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 200, 221 U.S.P.Q. 1125 (Fed. Cir. 1984); M.P.E.P. §2143.02.

operation of Tanioka.[12] Additionally, the proposed modification or combination of the Tanioka reference would render the operation of Tanioka unsatisfactory for its intended purpose and, therefore, the teachings of the reference are not sufficient to render the claims *prima facie* obvious. Applicants submit that, at least for the reasons above, the combination of Tanioka and DiStefano are improper and, therefore, the Office Action fails to establish a *prima facie* case of obviousness for independent claim 59.

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0441 or any payment in connection with this communication that may be required.

Applicants respectfully submit that the claims are in condition for allowance. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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[12] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); see M.P.E.P. §2143.01.